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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/838,057	04/19/2001	William Joseph Armstrong		8659

7590 07/29/2004

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EXAMINER	
NGUYEN, VAN H	

ART UNIT	PAPER NUMBER
2126	

DATE MAILED: 07/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/838,057	ARMSTRONG ET AL.	
	Examiner	Art Unit	
	VAN H NGUYEN	2126	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4/19/01, 7/15/02, 8/18/03, 10/20/03 and 1/16/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 are presented for examination.

2. The cross reference related to the application cited in the specification must be updated (i.e., update the relevant status, with patent numbers where appropriate, on the specification page 7). Correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A. The following phrases lack antecedent basis:

(i) said multi-processor system (claim 1, line 6)

(ii) said first set (claim 1, line 12)

(iii) the processor set (claim 1, line 15)

(iv) the set of central processing units (claim 5, line 14)

(v) said first set (claim 11, line 14)

(vi) the processor set (claim 11, line 18)

B. The phrase "central processing units" (claim 5, line 6) is indefinite because it is not clear if Applicant intends to refer it to "said central processing units " claimed in lines 4-5.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made
>
> This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Cameron et al.** (U.S. 5,325,526).

7. As to claim 1, Cameron teaches the invention substantially as claimed including a method for allocating processor resources in a computer system having a plurality of central processors (abstract and col.2, lines 28-47), comprising the steps of:

- defining a plurality of logical partitions of the computer system, wherein each task executing in the computer system is assigned to a respective one of the logical partitions (col.2, lines 48-65; col.7, lines 31-52; and col.24, lines 26-37);

- defining a plurality of sets of processors; assigning each central processor of the multi-processor system to a respective set of the plurality of processor sets (col.3, lines 10-16, and 62-67);

- assigning each logical partition of the plurality of logical partitions to a respective set of the plurality of processor sets, wherein a first processor set of the plurality of processor sets has a plurality of logical partitions assigned to it partitions (col.2, lines 51-53; col.3, lines 62-67; col.7, lines 31-52; and col.24, lines 26-31);

- assigning a respective processing capacity value to each of the plurality of logical partitions assigned to the first set, the capacity values representing processing capacity in units equivalent to a fixed number of physical central processors (col.10, lines 4-25);

- constraining tasks executing in a each logical partition to execute only in central processors assigned to the processor set to which the respective logical partition is assigned (col.3, lines 22-27 and col.8, lines 14-19); and

Cameron does not explicitly teach constraining tasks executing in the each logical partition assigned to the first processor set to execute for a combined length of time equivalent to the processing capacity value assigned to the respective logical partition.

Cameron, however, discloses "executing all tasks of said partition concurrently for a length of time no longer than a predetermined activation time period" (col.1, lines 53-59).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have included "constraining tasks executing in the each logical partition assigned to the first processor set to execute for a combined length of time equivalent to the processing capacity value assigned to the respective logical partition" because this will provide an optimal execution environment for the execution of a plurality of tasks in a multicomputer.

8. As to claim 2, Cameron teaches designating each respective logical partition assigned to the first processor set as either capped or uncapped; wherein, with respect to a logical partition which is designated capped, the step of constraining tasks executing in the logical partition to execute for a combined length of time equivalent to the processing capacity value comprises preventing tasks in the partition from executing if the processing capacity value has been reached (col.5, line 58-col.6, line 7); and wherein, with respect to a logical partition which is designated uncapped, the step of constraining tasks executing in the logical partition to execute for a combined length of time equivalent to the processing capacity value comprises preventing tasks in the partition from executing if the processing capacity value has been reached, unless there is unused processing capacity in the first processor set (col.6, lines 12-21).

9. As to claim 3, Cameron teaches assigning a respective number of virtual processors to each of the plurality of logical partitions assigned to the first processor set (col.8, line 63-col.7, line 5).

10. As to claim 4, Cameron teaches a second processor set of the plurality of processor sets has a plurality of logical partitions assigned to it (col.3, lines 62-66), the method further comprising: assigning a respective processing capacity value to each of the plurality of logical partitions assigned to the second set, the capacity values representing processing capacity in units

equivalent to a fixed number of physical central processors (col.10, lines 4-25). Refer to the discussion of claim 1 above for rejection of "constraining tasks executing in the each logical partition assigned to the second processor set to execute for a combined length of time equivalent to the processing capacity value assigned to the respective logical partition."

11. As to claim 9, Cameron teaches altering a processor capacity value of a first logical partition assigned to the first set, while holding a processor capacity value of a second logical partition assigned to the first set constant (col.14, lines 12-32).

12. As to claim 10, Cameron teaches at least one processor set of the plurality of processor sets has only a single logical partition assigned to it (col.2, lines 48-58).

13. As to claim 5, note the rejection of claim 1 above. Claim 5 is the same as claim 1, except claims 5 is a system claim and claim 1 is method claim.

14. As to claim 6, Cameron teaches each logical partition contains a respective task dispatching function; wherein the logical partitioning enforcement function comprises a respective low-level virtual processor dispatcher for each set of central processing units operating below the level of the task dispatching functions, the task dispatching functions dispatching tasks to virtual processors, the virtual processor dispatchers dispatching the virtual processors to the central processing units (col.2, lines 59-65 and col.7, lines 29-42).

15. As to claim 7, it includes the same subject matter as in claim 2 above, and is similarly rejected under the same rationale.

16. As to claim 8, Cameron teaches with respect to multiple logical partitions assigned to a single central processing unit set, the logical partitioning configuration function further receives a user designation of a respective number of virtual processors for each such logical partitions;

and wherein the logical partitioning enforcement mechanism limits simultaneous execution of tasks of a logical partition of multiple logical partitions assigned to a single central processing unit set to the number of virtual processors assigned to the logical partition (col.24, lines 20-39).

17. As to claims 11-16, note the rejection of claims 1-4 and 9-10 above. Claims 11-16 are the same as claims 1-4 and 9-10, except claims 11-16 are computer program product claims and claims 1-4 and 9-10 are method claims.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Zalewski et al. (U.S. 6647508) teaches "Multiprocessor computer architecture with multiple operating system instances and software controlled resource allocation."

- Rooney et al. (U.S. 6598069) teaches "Method and apparatus for assigning resources to logical partition clusters."

- Zalewski et al. (U.S. 6542926) teaches "Software partitioned multi-processor system with flexible resource sharing levels."

- Kleinsorge et al. (U.S. 6247019) teaches "Dynamically assigning CPUs to different partitions each having an operation system instance in a shared memory space."

- Yokoya (U.S. 6199093) teaches "Processor allocating method/apparatus in multiprocessor system, and medium for storing processor allocating program."

- Hancock et al. (U.S. 5574914) teaches "Method and apparatus for performing system resource partitioning."

- Pian et al. (U.S. 5357632) teaches "Dynamic task allocation in a multi-processor system employing distributed control processors and distributed arithmetic processors."

- Bakshi "Partitioning and pipelining for performance-constrained hardware/software systems" 1999 IEEE, pp.419-432.

- Ayachi et al. "A hierarchical processor scheduling policy for multiprocessor systems" 1996 IEEE, pp.100-109.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VAN H NGUYEN whose telephone number is (703) 306-5971. The examiner can normally be reached on Monday-Thursday from 8:30AM - 6:00PM. The examiner can also be reached on alternative Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (703) 305-9678.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VHN

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